



## APPLICABILITY TABLE

PRODUCT
GL865-DUAL V3
GL865-QUAD V3
GL865-DUAL V3.1
GL865-QUAD V3.1





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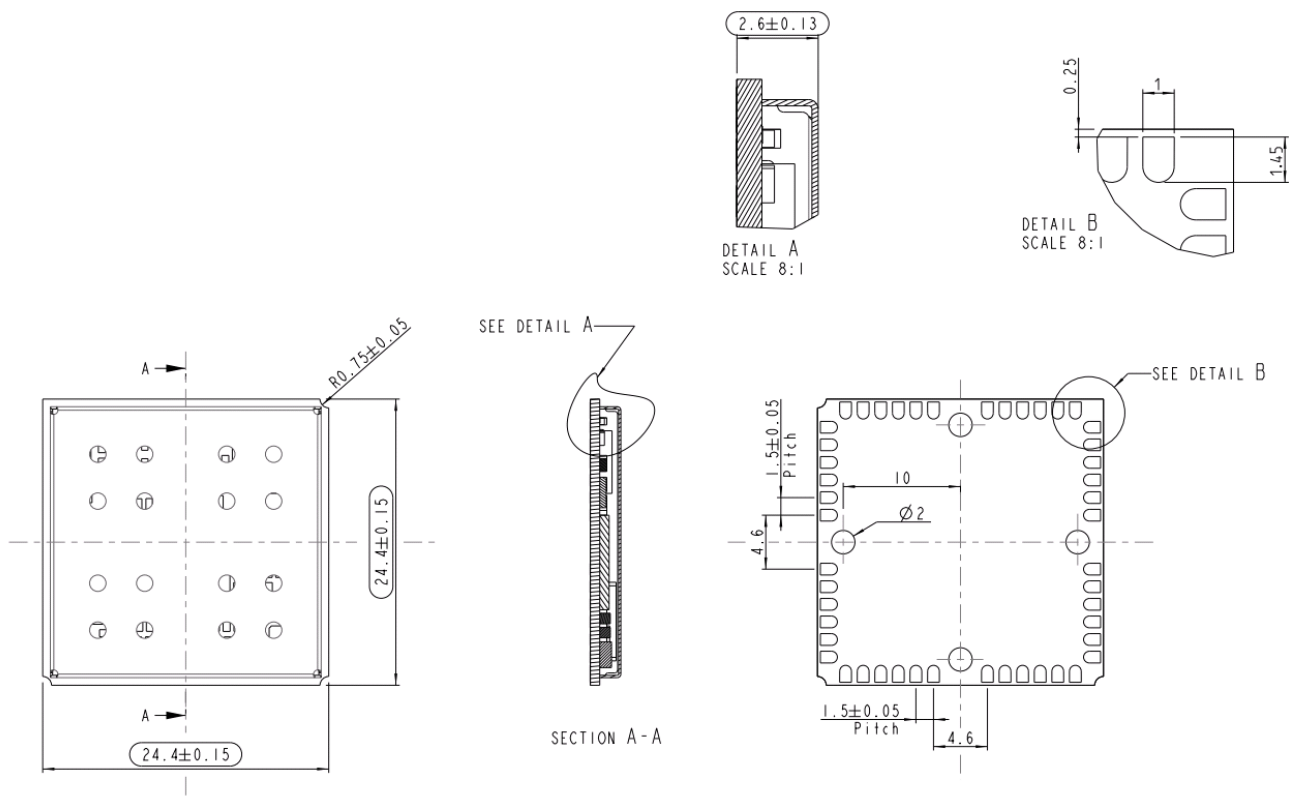




### 3. GL865 V3/V3.1 Mechanical Dimensions

The GL865 V3/V3.1 overall dimensions are:

- Length: 24.4 mm
- Width: 24.4 mm
- Thickness: 2.6 mm
- Weight: 2.8 g





Pad	Signal	I/O	Function	Note	Type
<b>GPIO</b>					
42	GPIO_01 / DVI_WA0	I/O	GPIO01 Configurable GPIO / Digital Audio Interface (WA0)	80KΩ- 110KΩ PD	CMOS 1.8V
41	GPIO_02 / JDR / DVI_RX	I/O	GPIO02 I/O pin / Jammer Detect Report / Digital Audio Interface (RX)	18KΩ- 25KΩ PD	CMOS 1.8V
40	GPIO_03 / DVI_TX	I/O	GPIO03 GPIO I/O pin / Digital Audio Interface (TX)	80KΩ- 110KΩ PD	CMOS 1.8V
39	GPIO_04 / TX Disable / DVI_CLK	I/O	GPIO04 Configurable GPIO / TX Disable input / Digital Audio Interface (CLK)	18KΩ- 25KΩ PD	CMOS 1.8V
29	GPIO_05 / RFTXMON	I/O	GPIO05 Configurable GPIO / Transmitter ON monitor	28KΩ- 40KΩ PD	CMOS 1.8V
28	GPIO_06 / ALARM	I/O	GPIO06 Configurable GPIO / ALARM	28KΩ- 40KΩ PD	CMOS 1.8V
27	GPIO_07 / BUZZER	I/O	GPIO07 Configurable GPIO / Buzzer	28KΩ- 40KΩ PD	CMOS 1.8V
26	GPIO_08 / STAT_LED	I/O	GPIO08 Configurable GPIO / Status LED	28KΩ- 40KΩ PD	CMOS 1.8V
<b>Power Supply</b>					
38	VBATT	-	Main power supply (Baseband)		Power
37	VBATT_PA	-	Main power supply (Radio PA)		Power
23	AGND	-	AF Signal Ground (see audio section)		AF Signal
32	GND	-	Ground		Power
33	GND	-	Ground		Power
35	GND	-	Ground		Power
36	GND	-	Ground		Power
46	GND	-	Ground		Power
<b>RESERVED</b>					
48		-			
16		-			
17		-			
18		-			
19		-			
25		-			
31		-			



**WARNING:**

Reserved pins must not be connected.







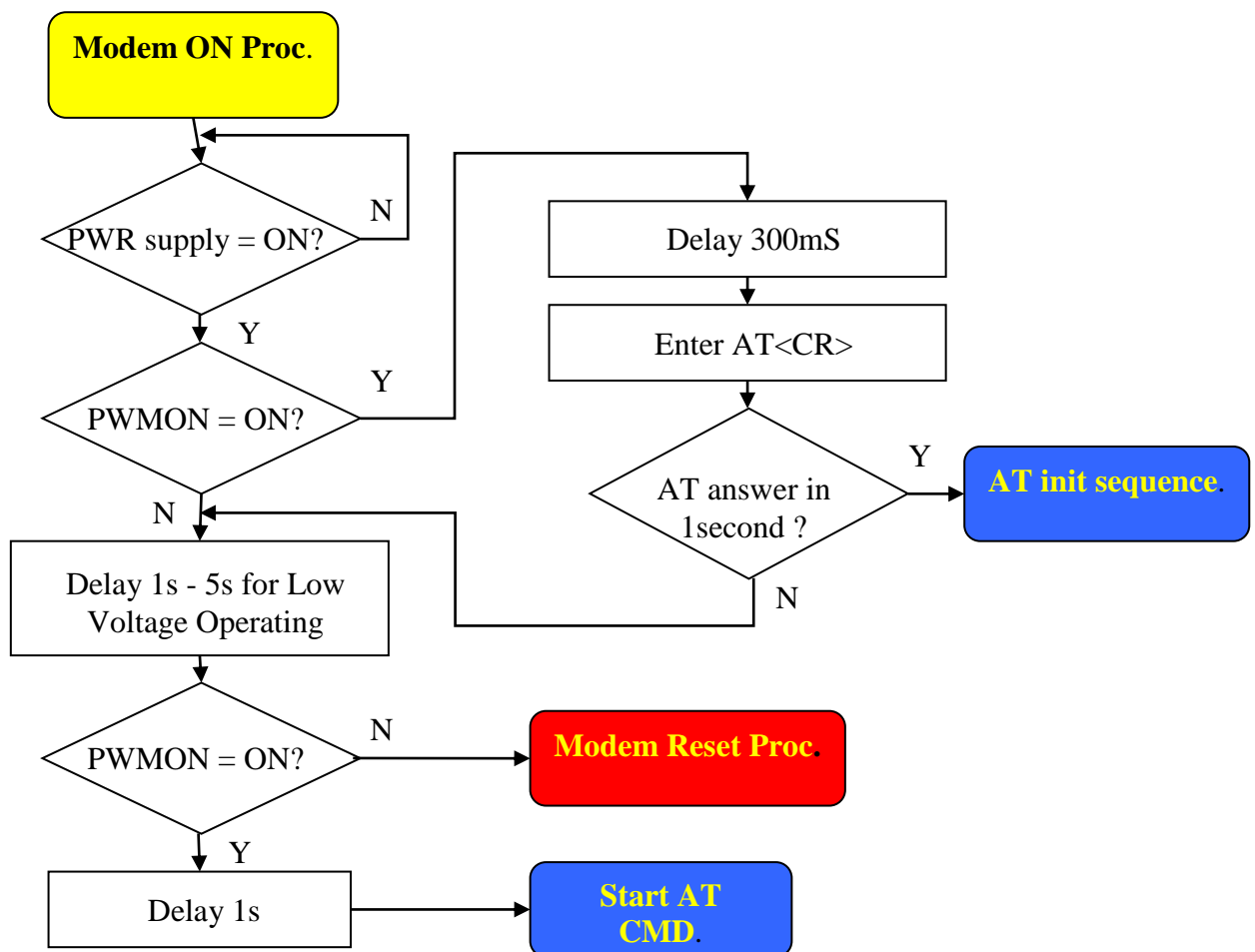
## 5. Hardware Commands

### 5.1. Auto-Turning ON the GL865 V3/V3.1

To Auto-turn on the GL865 V3/V3.1, the power supply must be applied on the power pins VBATT and VBATT\_PA, after 1000 m-seconds, the V\_AUX / PWRMON pin will be at the high logic level and the module can be considered fully operating.

When the power supply voltage is between 3.22V and 3.4V, after 5000 m-seconds, the V\_AUX / PWRMON pin will be at the high logic level and the module can be considered fully operating.

The following flow chart shows the proper turn on procedure:



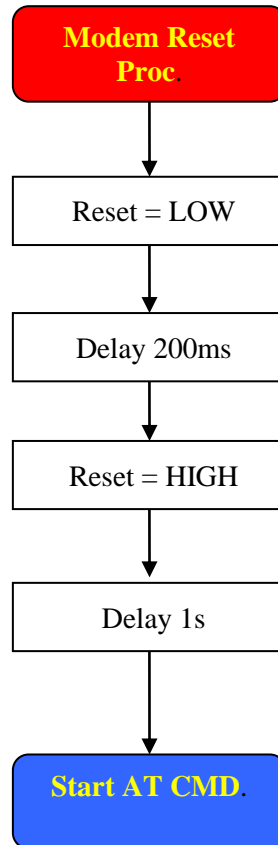








In the following flow chart is detailed the proper restart procedure:



**NOTE:**

In order to prevent a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the GL865 V3/V3.1 when the module is powered OFF or during an ON/OFF transition.



## 6. Power Supply

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performance, hence read the requirements carefully and the guidelines that will follow for a proper design.

### 6.1. Power Supply Requirements

The external power supply must be connected to VBATT & VBATT\_PA signals and must fulfill the following requirements:

POWER SUPPLY	
Nominal Supply Voltage	3.8 V
Normal Operating Voltage Range	3.40 V ÷ 4.20 V
Extended Operating Voltage Range	3.10 V ÷ 4.50 V



**NOTE:**

The Operating Voltage Range **MUST** never be exceeded; care must be taken when designing the application's power supply section to avoid having an excessive voltage drop.

If the voltage drop is exceeding the limits it could cause a Power Off of the module.

The Power supply must be higher than 3.22 V to power on the module.



**NOTE:**

Overshoot voltage (regarding MAX Extended Operating Voltage) and drop in voltage (regarding MIN Extended Operating Voltage) **MUST** never be exceeded;

The "Extended Operating Voltage Range" can be used only with complete assumption and application of the HW User guide suggestions.



**NOTE:**

When the power supply voltage is between 3.22V and 3.4V, after 5000 m-seconds, the V\_AUX / PWRMON pin will be at the high logic level and the module can be consider fully operating. See Par. 5.1.



## 6.2. Power Consumption

The GL865 V3/V3.1 power consumptions are:

GL865 V3/V3.1		
Mode	Average (mA)	Mode description
<b>SWITCHED OFF</b>		
Switched Off	Typical 2uA max 20uA	Module power supplied only on VBATT_PA pin, the VBATT pin is not power supplied.
Switched Off with AT#SYSHALT	<500uA	
<b>IDLE mode</b>		
AT+CFUN=1	9	Normal mode: full functionality of the module
AT+CFUN=4	9	Disabled TX and RX; module is not registered on the network
AT+CFUN=0 or =5	1.7	Paging Multiframe 2
	1.5	Paging Multiframe 3
	1,3	Paging Multiframe 4
	0,8	Paging Multiframe 9
<b>CSD TX and RX mode</b>		
GSM900 CSD PL5	200	GSM VOICE CALL
DCS1800 CSD PL0	150	
<b>GPRS (class 1) 1TX + 1RX</b>		
GSM900 PL5	200	GPRS Sending data mode
DCS1800 PL0	140	
<b>GPRS (class 10) 2TX + 3RX</b>		
GSM900 PL5	300	GPRS Sending data mode
DCS1800 PL0	250	

The GSM system is made in a way that the RF transmission is not continuous, but it is packed into bursts at a base frequency of approx. 217 Hz, and the relative current peaks can be as high as about 2A. Therefore the power supply has to be designed to withstand these current peaks without big voltage drops; this means that both the electrical design and the board layout must be designed for this current flow.

If the layout of the PCB is not well designed a strong noise floor is generated on the ground and the supply; this will reflect on all the audio paths producing an audible annoying noise at approx. 217 Hz; if the voltage drop during the peak current absorption is too much, then the device may even shutdown as a consequence of the supply voltage drop.



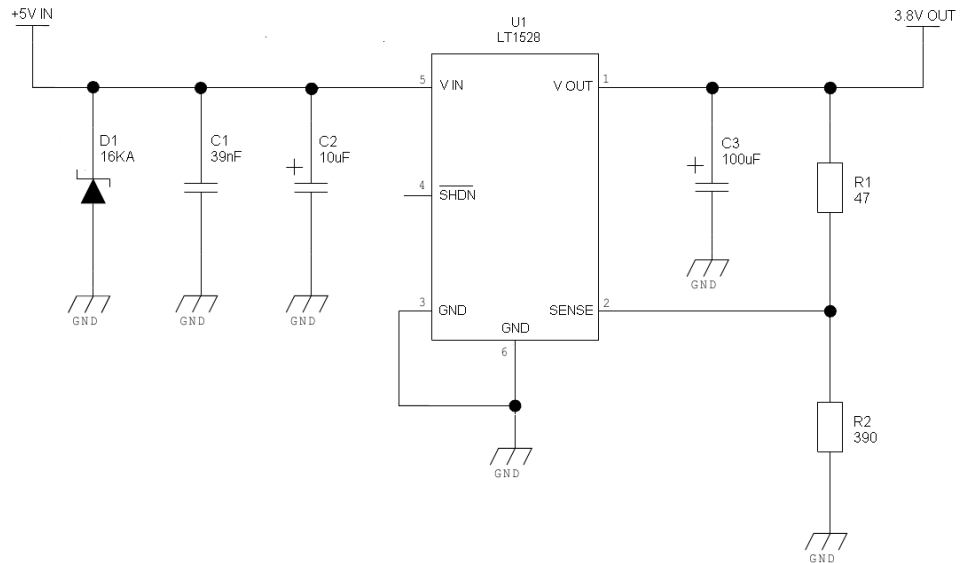
### NOTE:

The electrical design for the Power supply should be made ensuring it will be capable of a peak current output of at least 2 A.





An example of linear regulator with 5V input is:



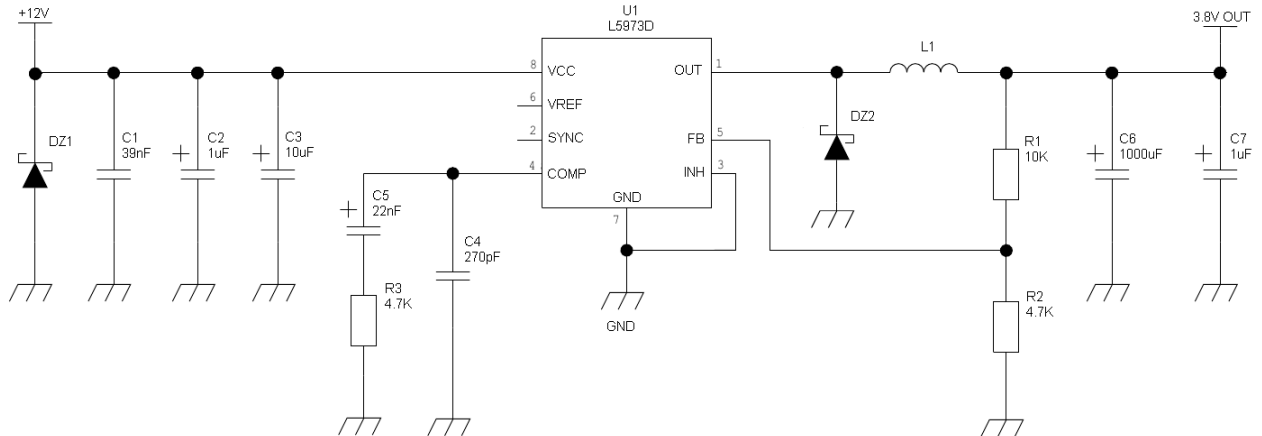
6.3.1.2.

#### + 12V input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching power supply will be preferable because of its better efficiency especially with the 2A peak current load represented by the GL865 V3/V3.1.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and Switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15,8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For Car applications a spike protection diode should be inserted close to the power input, in order to clean the supply from spikes.
- A protection diode should be inserted close to the power input, in order to save the GL865 V3/V3.1 from power polarity inversion. This can be the same diode as for spike protection.



An example of switching regulator with 12V input is in the below schematic:



6.3.1.3.

### Battery Source Power Supply Design Guidelines

- The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V, hence a single 3.7V Li-Ion cell battery type is suited for supplying the power to the Telit GL865 V3/V3.1 module.



#### WARNING:

The three cells Ni/Cd or Ni/MH 3.6 V Nom. battery types or 4V PB types **MUST NOT BE USED DIRECTLY** since their maximum voltage can rise over the absolute maximum voltage for the GL865 V3/V3.1 and damage it.



#### NOTE:

DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with GL865 V3/V3.1. Their use can lead to overvoltage on the GL865 V3/V3.1 and damage it. USE ONLY Li-Ion battery types.

- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the GL865 V3/V3.1 from power polarity inversion. Otherwise the battery connector should be done in a way to avoid polarity inversions when connecting the battery.
- The battery capacity must be at least 500mAh in order to withstand the current peaks of 2A; the suggested capacity is from 500mAh to 1000mAh.



## 6.3.2. Thermal Design Guidelines

The thermal design for the power supply heat sink should be done with the following specifications:

See Par. 6.2 Power Consumption



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### NOTE:

The average consumption during transmissions depends on the power level at which the device is requested to transmit by the network. The average current consumption hence varies significantly.

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Considering the very low current during idle, especially if Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.

For the heat generated by the GL865 V3/V3.1, you can consider it to be during transmission 1W max during CSD/VOICE calls and 2W max during class10 GPRS upload.

This generated heat will be mostly conducted to the ground plane under the GL865 V3/V3.1; you must ensure that your application can dissipate it.









## 7.2. PCB Design Guidelines

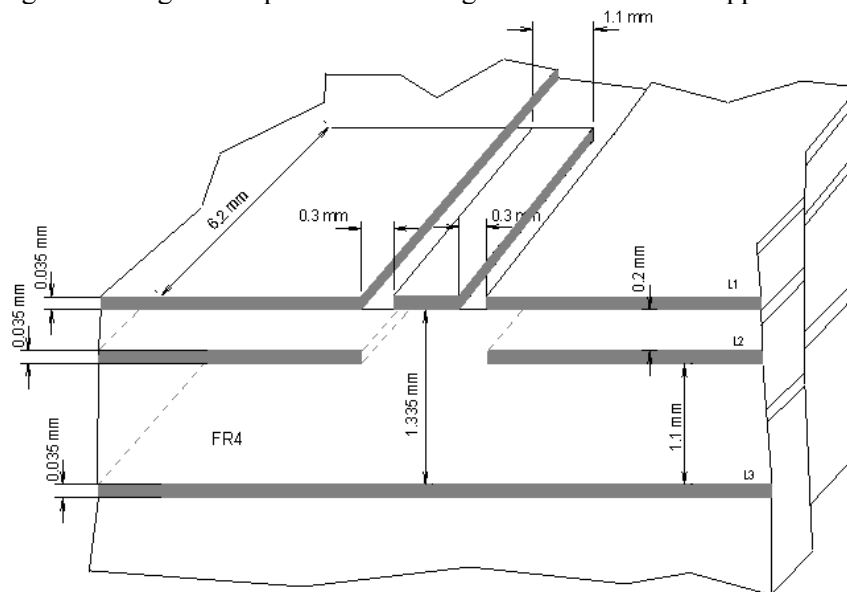
This section explains the suggested design for the transmission line on the customer's application board.

### 7.2.1. Transmission line design

During the design of the GL865 V3/V3.1 interface board (see the Telit EVK2 User Guide, 1vv0300704), the placement of components has been chosen properly, in order to keep the line length as short as possible, thus leading to lowest power losses possible. A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. A SMA female connector has been used to feed the line.

The interface board is realized on a FR4, 4-layers PCB. Substrate material is characterized by relative permittivity  $\epsilon_r = 4.6 \pm 0.4 @ 1 \text{ GHz}$ ,  $\text{TanD} = 0.019 \div 0.026 @ 1 \text{ GHz}$ .

A characteristic impedance of nearly  $50 \Omega$  is achieved using trace width = 1.1 mm, clearance from coplanar ground plane = 0.3 mm each side. The line uses reference ground plane on layer 3, while copper is removed from layer 2 underneath the line. Height of trace above ground plane is 1.335 mm. Calculated characteristic impedance is  $51.6 \Omega$ , estimated line loss is less than 0.1 dB. The line geometry shown below is just an example and the values may change according to the specific PCB design on the customer's application board:



#### NOTE:

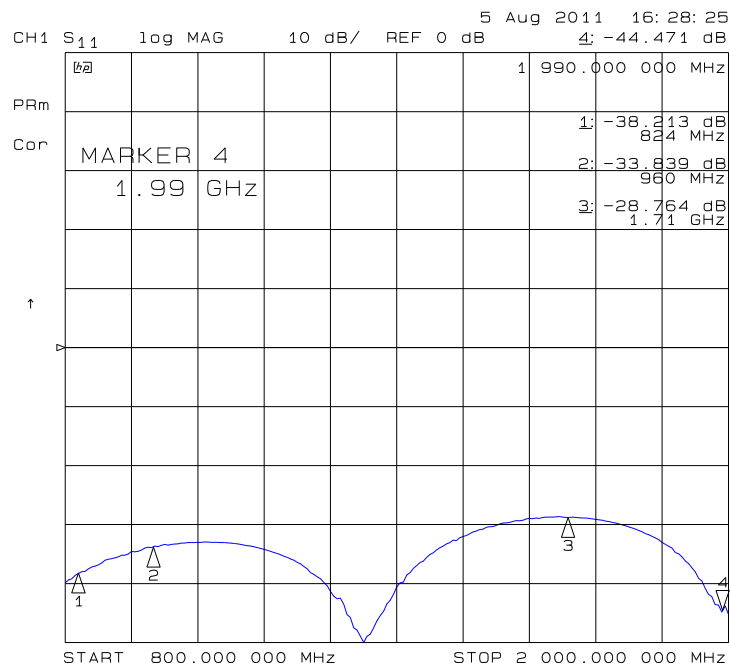
Please refer to Telit modem integration design guide 1VV0301189 for further details.



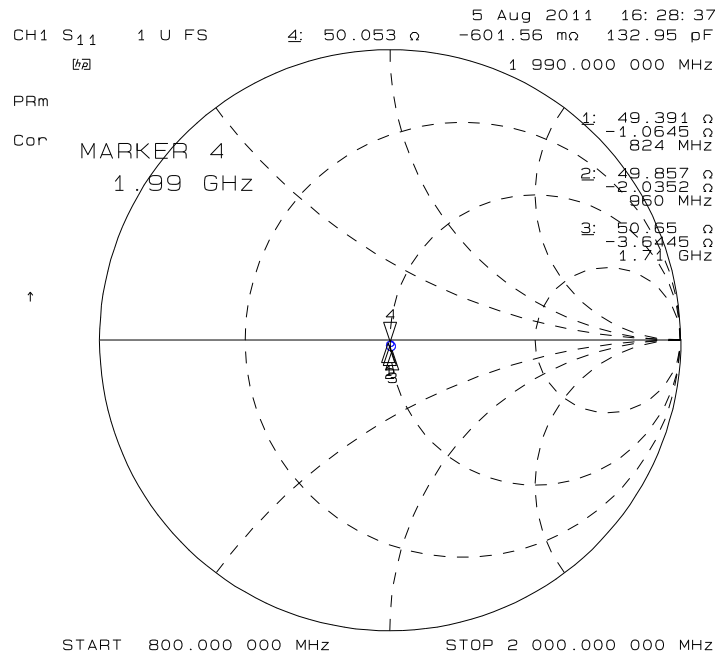
## Transmission line measurements

HP8753E VNA (Full-2-port calibration) has been used in this measurement session. A calibrated coaxial cable has been soldered at the pad corresponding to GL865 V3/V3.1 RF output; a SMA connector has been soldered to the board in order to characterize the losses of the transmission line including the connector itself. During Return Loss / impedance measurements, the transmission line has been terminated to 50  $\Omega$  load.

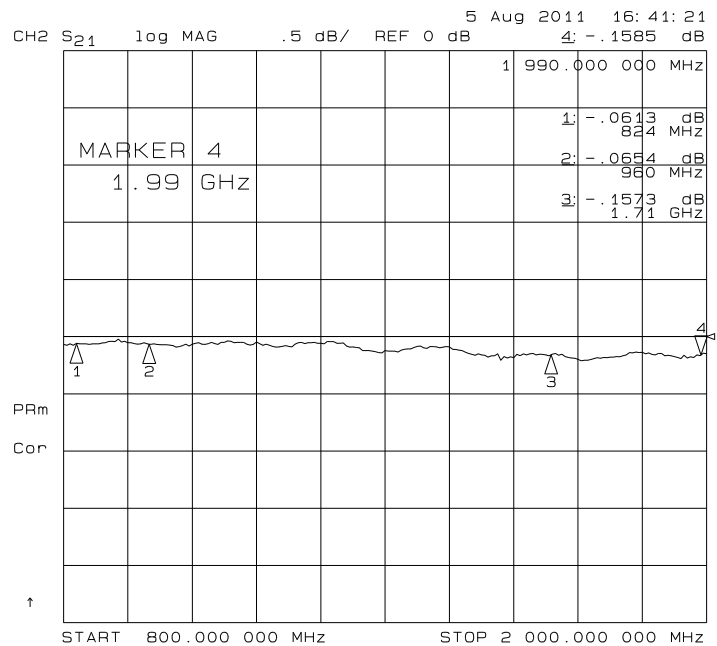
Return Loss plot of line under test is shown below:



Line input impedance (in Smith Chart format, once the line has been terminated to 50  $\Omega$  load) is shown in the following figure:



Insertion Loss of G-CPW line plus SMA connector is shown below:



### 7.3. GSM Antenna - Installation Guidelines

- Install the antenna in a place covered by the GSM signal.
- Antenna shall not be installed inside metal cases
- Antenna shall be installed also according to antenna manufacturer instructions.
- Installation should also take in account the R&TTE requirements described in the “Conformity Assessment Issues” chapter



## 8. Logic level specifications

Where not specifically stated, all the interface circuits work at 1.8V CMOS logic levels. The following table shows the logic level specifications used in the GL865 V3/V3.1 interface circuits:

### Absolute Maximum Ratings -Not Functional

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) when on	-0.3V	+2.1V

### Operating Range - Interface levels (1.8V CMOS)

Level	Min	Max
Input high level	1.3V	1.9V
Input low level	0V	0.35V
Output high level	1.6V	1.9V
Output low level	0V	0.2V

### Current characteristics

Level	Typical
Output Current	1mA
Input Current	1uA



## 8.1. Reset signal

Signal	Function	I/O	pin
RESET*	Phone reset	I	47

RESET\* is used to reset the GL865 V3/V3.1. Whenever this signal is pulled low, the GL865 V3/V3.1 is reset. When the device is reset it stops any operation. After the release of the reset GL865 V3/V3.1 is unconditionally shut down, without doing any detach operation from the network where it is registered. This behavior is not a proper shut down because any GSM device is requested to issue a detach request on turn off. For this reason the Reset signal must not be used to normally shutting down the device, but only as an emergency exit in the rare case the device remains stuck waiting for some network response.

The RESET\* is internally controlled on start-up to achieve a proper power-on reset sequence, so there's no need to control this pin on start-up. It may only be used to reset a device already on that is not responding to any command.



### NOTE:

Do not use this signal to power OFF the GL865 V3/V3.1. Use the ON/OFF procedure to perform this function.

### Reset Signal Operating levels:

Signal	Min	Max
RESET* Input high	1.8V(NOTE1)	2.1V
RESET* Input low	0V	0.2V

(NOTE1) this signal is internally pulled up so the pin can be left floating if not used.

If unused, this signal may be left unconnected. If used, then it must always be connected with an open collector transistor, to permit to the internal circuitry the power on reset and under voltage lockout functions.



## 9. Serial Ports

The serial port on the GL865 V3/V3.1 is the core of the interface between the module and OEM hardware.

2 serial ports are available on the module:

- MODEM SERIAL PORT 1 (Main, ASC0)
- MODEM SERIAL PORT 2 (Auxiliary, ASC1)

### 9.1. MODEM SERIAL PORT

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:

- RS232 PC com port
- microcontroller UART @ 1.8V (Universal Asynchronous Receive Transmit)
- microcontroller UART @ 3V or other voltages different from 1.8V
- microcontroller UART @ 5V or other voltages different from 1.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work. The only configuration that doesn't need a level translation is the 1.8V UART.

The serial port on the GL865 V3/V3.1 is a +1.8V UART with all the 8 RS232 signals. It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels. The levels for the GL865 V3/V3.1 UART are the CMOS levels:

**Absolute Maximum Ratings -Not Functional**

Parameter	Min	Max
Input level on any digital pad when on	-0.3V	+2.1V
Input voltage on analog pads when on	-0.3V	+2.1V

**Operating Range - Interface levels (1.8V CMOS)**

Level	Min	Max
Input high level $V_{IH}$	1.5V	1.9V
Input low level $V_{IL}$	0V	0.35V
Output high level $V_{OH}$	1.6V	1.9V
Output low level $V_{OL}$	0V	0.2V



The signals of the GL865 V3/V3.1 serial port are:

RS232 Pin Number	Signal	GL865 V3/V3.1 Pad Number	Name	Usage
1	DCD - dcd_uart	1	Data Carrier Detect	Output from the GL865 V3/V3.1 that indicates the carrier presence
2	RXD - tx_uart	8	Transmit line *see Note	Output transmit line of GL865 V3/V3.1 UART
3	TXD - rx_uart	7	Receive line *see Note	Input receive of the GL865 V3/V3.1 UART
4	DTR - dtr_uart	4	Data Terminal Ready	Input to the GL865 V3/V3.1 that controls the DTE READY condition
5	GND	32, 33, 35, 36, 46	Ground	Ground
6	DSR - dsr_uart	3	Data Set Ready	Output from the GL865 V3/V3.1 that indicates the module is ready
7	RTS -rts_uart	5	Request to Send	Input to the GL865 V3/V3.1 that controls the Hardware flow control
8	CTS - cts_uart	6	Clear to Send	Output from the GL865 V3/V3.1 that controls the Hardware flow control
9	RI - ri_uart	2	Ring Indicator	Output from the GL865 V3/V3.1 that indicates the incoming call condition



**NOTE:**

According to V.24, RX/TX signal names are referred to the application side, therefore on the GL865 V3/V3.1 side these signal are on the opposite direction: TXD on the application side will be connected to the receive line (here named TXD/ rx\_uart ) of the GL865 V3/V3.1 serial port and vice versa for RX.



**NOTE:**

For a minimum implementation, only the TXD and RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.



**NOTE:**

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the GL865 V3/V3.1 when the module is powered off or during an ON/OFF transition.



## 9.2. RS232 level translation

In order to interface the GL865 V3/V3.1 with a PC com port or a RS232 (EIA/TIA-232) application a level translator is required. This level translator must:

- invert the electrical signal in both directions;
- change the level from 0/1.8V to +15/-15V

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.

The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).

By convention the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART.

In order to translate the whole set of control lines of the UART you will need:

- 5 drivers
- 3 receivers



---

### NOTE:

The digital input lines working at 1.8V CMOS have an absolute maximum input voltage of 2.1V; therefore the level translator IC shall not be powered by the +3.8V supply of the module. Instead, it must be powered from a +1.8V (dedicated) power supply.

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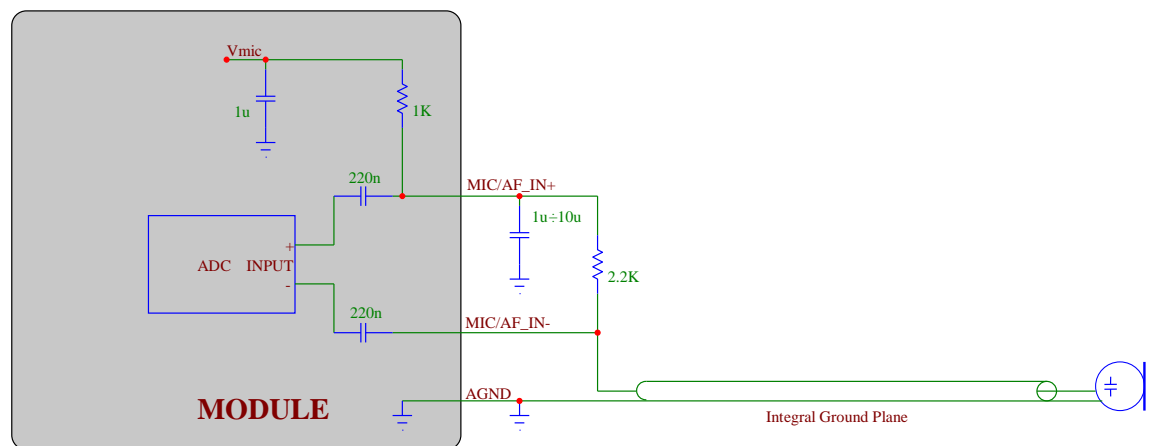


## 10. Audio Section Overview

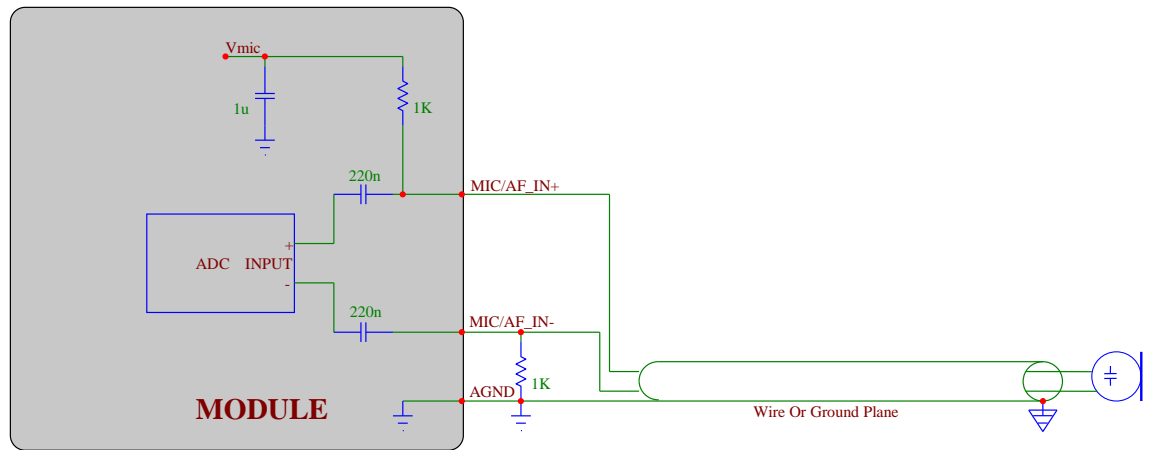
The Base Band Chip of the GL865 V3/V3.1 provides one input for audio to be transmitted (*Uplink*) that can be connected directly to a microphone or an audio source. The bias for the microphone is already provided by the product; so the connection can be done in both following ways:

### 10.1. MIC connection

The first connection (referred to as single ended) is preferable, since the residual  $V_{mic}$  noise is fed into the input as common mode and therefore rejected, while the ground noise is blocked by the high impedance of the microphone (electret mike is a current signal source). In this situation we have to recall that the microphone is a sound to current transducer, so the resistor turns the current into voltage and acts as a voltage source; finally the resistor feeds the input in balanced way even if the configuration, from a microphone point of view, seems to be un-balanced.

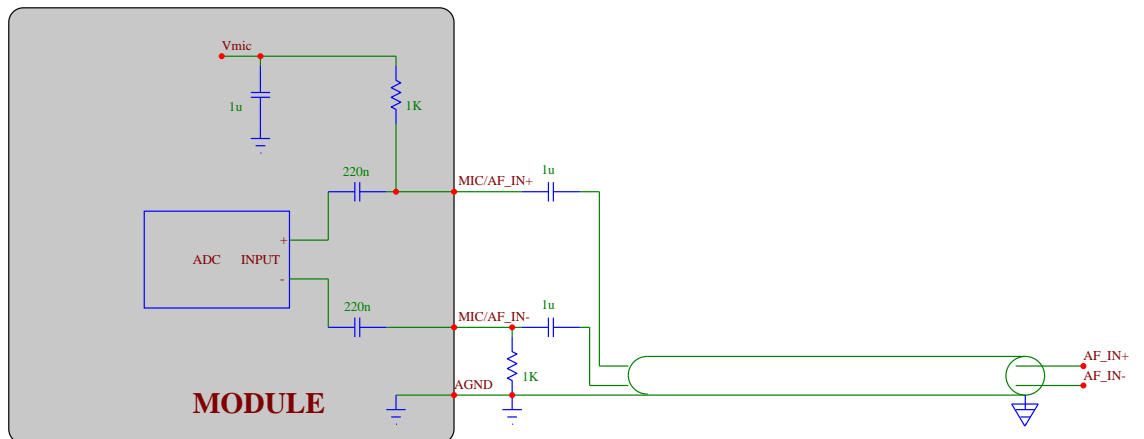


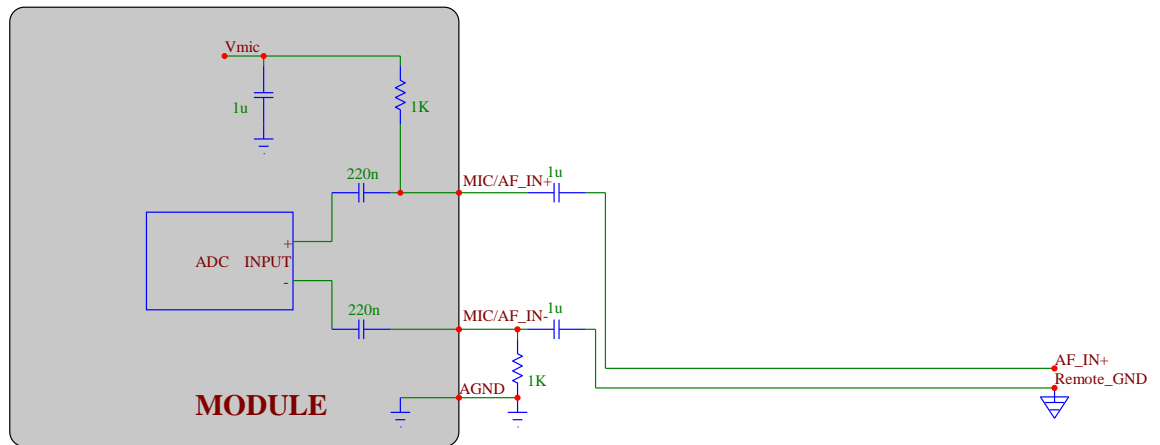
If a "balanced way" is anyway desired, much more care has to be taken to  $V_{mic}$  noise and ground noise; also the 33pF-100Ω-33pF RF-filter has to be doubled (one each wire).



**TIP:** Since the J-FET transistor inside the microphone acts as RF-detector-amplifier, ask vendor for a microphone with anti-EMI capacitor (usually a 33pF or a 10pF capacitor placed across the output terminals inside the case).

## 10.2. LINE-IN connection

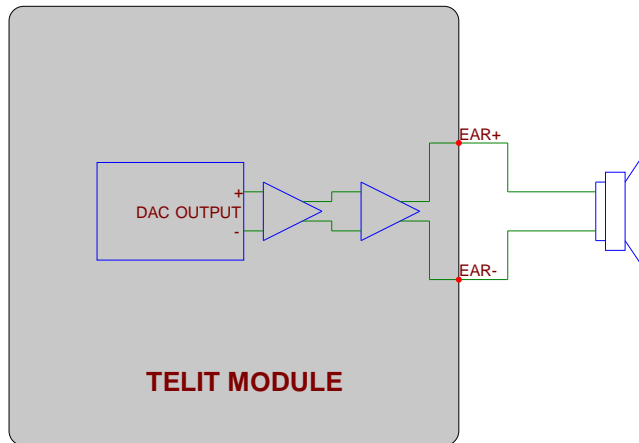




If the audio source is not a mike but a different device, the following connections can be done. Place a  $1K\Omega$  resistor to ground on the negative input, in order to get balanced the input; than connect the source via  $1\mu F$  capacitor, so the DC current is blocked. Since the input is differential, the common mode voltage noise between the two (different) grounds is rejected, provided that both AF\_IN+ & AF\_IN- are connected directly onto the source.



### 10.3. EAR connection



The audio output of the GL865 V3/V3.1 is balanced, this is helpful to double the level and to reject common mode (click and pop are common mode and therefore rejected); furthermore the output stage is class-D, so it can manage directly a loudspeaker with electrical impedance of at least  $8\Omega$ . This stage is powered by switching from  $V_{batt}$  to  $gnd$  at a frequency ranging from 0.6 to 2MHz, so it has a good efficiency and thus a big power budget; being a class-D architecture, please use some caution (see the NOTE below).



**NOTE:**

When the loudspeaker is connected with a long cable, an L-C filter is recommended.  
When the EAR+/- are feeding some electronic circuitry, an R-C filter is recommended.



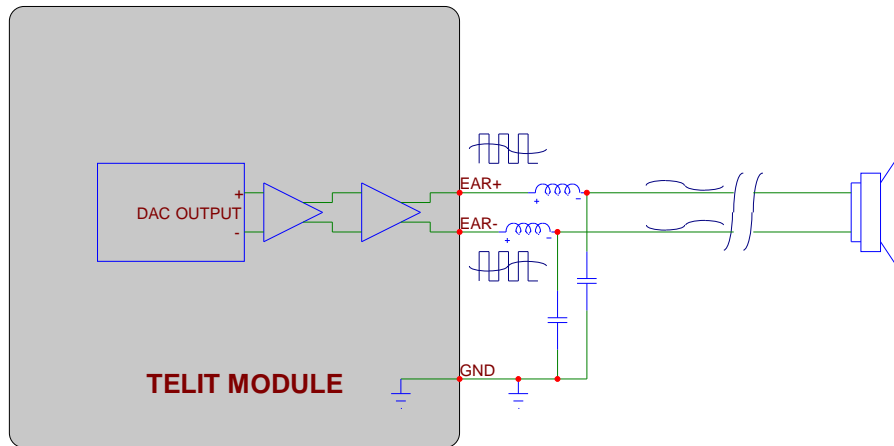
**TIP:** in order to get the maximum audio level at a given output voltage level (dBspl/Vrms), the following breaking through procedure can be used. Have the loudspeaker as close as you can to the listener (this simplify also the echo cancelling); choose the loudspeaker with the higher sensitivity (dBspl per W); choose loudspeakers with the impedance close to the limit (ex: 16 or  $8\Omega$ ), in order to feed more power inside the transducer (it increases the W/Vrms ratio). If this were not enough, an external amplifier should be used.



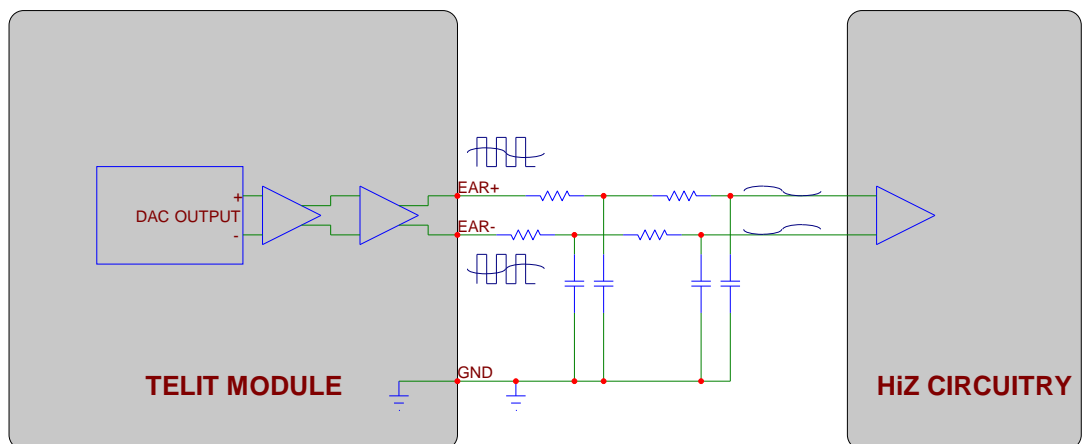
**WARNING:**

The audio output hardware of the GL865 V3/V3.1 is based on a Class-D amplifier so any singled-end output configuration **MUST NOT BE USED**, otherwise the presence of GSM buzzing and low level audio performance will result.





L-C filtering for LOW impedance load.



R-C filtering for HIGH impedance load.



## 10.4. Electrical Characteristics

### 10.4.1. Input Lines

Microphone/Line-in path	
Line Type	Differential
Coupling capacitor	$\geq 100\text{nF}$
Differential input resistance	$50\text{k}\Omega$
Levels	
To have 0 dBfs @1KHz (*)	Differential input voltage
MIC Gain = 0dB	290mVrms
MIC Gain = +6dB	145mVrms
MIC Gain = +12dB	72mVrms
MIC Gain = +18dB	36mVrms
MIC Gain = +24dB	18mVrms
MIC Gain = +30dB	9mVrms
MIC Gain = +36dB	4.5mVrms
MIC Gain = +42dB	2.25mVrms

(\*) 0 dBfs in the network are +3.14 dBm0



**TIP:** The Electret microphone is internally amplified by a J-Fet transistor, thus the sound is carried out as saturation drain current; this means that the Norton equivalence has to be considered. The signal is converted to voltage on the  $2.2\text{K}\Omega$  resistance, from there on circuitry has to be routed in order to not pick up common mode noise; beware of the return path (ground).



## 10.4.2. Output Lines

EAR/Line-out Output	
Differential line coupling	Direct connection ( $V_{DC}=1.7\div 2.1V$ )
output load resistance	$\geq 8 \Omega$
signal bandwidth	250÷3400Hz (@ -3dB with default filter)
max. differential output voltage	1120 mV <sub>pp</sub> @3.14dBm0 (*)
differential output voltage	550mV <sub>rms</sub> @0dBm0 (*)
volume increment	2dB per step
volume steps	0..10

(\*) in default condition: Output Volume = +20dB, Output Attenuation = 0dB



**TIP:** We suggest driving the load differentially; this kills all the common mode noises (click and pop, for example), the output swing will double (+6dB) and the big output coupling capacitor will be avoided.

In order to get the maximum power output from the device, the resistance of the tracks has to be negligible in comparison to the load.



## 11. General Purpose I/O

The general purpose I/O pads can be configured to act in three different ways:

- input
- output
- alternate function (*internally controlled*)

*Input pads* can be read; they report the digital value (*high or low*) present on the pad at the read time .

*Output pads* can only be written or queried and set the value of the pad output.

An *alternate function pad* is internally controlled by the GL865 V3/V3.1 firmware and acts depending on the function implemented.

For Logic levels please refer to chapter 8.

The following table shows the available GPIO on the GL865 V3/V3.1.

Pin	Signal	I/O	Function	Type	Input / output current	Default State	ON_OFF state	State during Reset	Note
42	GPIO_01	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function DVI_WA0
41	GPIO_02	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function JDR and DVI_RX
40	GPIO_03	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function DVI_TX
39	GPIO_04	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function TX Disable and DVI_CLK
29	GPIO_05	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function RFTXMON
28	GPIO_06	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function ALARM
27	GPIO_07	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function BUZZER
26	GPIO_08	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function STAT_LED



### WARNING:

During power up the GPIOs may be subject to transient glitches.





## 11.2. Using a GPIO Pad as INPUT

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO.

If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 1.8V CMOS, then it can be buffered with an open collector transistor with a 47K pull up to 1.8V.



### NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the GL865 V3/V3.1 when the module is powered OFF or during an ON/OFF transition.



### TIP:

The V\_AUX / PWRMON pin can be used for input pull up reference or/and for ON monitoring.

## 11.3. Using a GPIO Pad as OUTPUT

The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

## 11.4. Using the RF Transmission Control GPIO4

The GPIO4 pin, when configured as RF Transmission Control Input, permits to disable the Transmitter when the GPIO is set to Low by the application.

In the design is necessary to add a resistor 47K pull up to 1.8V, this pull up must be switched off when the module is in off condition.

## 11.5. Using the RFTXMON Output GPIO5

The GPIO5 pin, when configured as RFTXMON Output, is controlled by the GL865 V3/V3.1 module and will rise when the transmitter is active and fall after the transmitter activity is completed.

There are 2 different modes for this function:

### 1) Active during all the Call:

For example, if a call is started, the line will be HIGH during all the conversation and it will be again LOW after hanged up.

The line rises up 300ms before first TX burst and will become again LOW from 500ms to 1s after last TX burst.



2) **Active during all the TX activity:**  
The GPIO is following the TX bursts

Please refer to the AT User interface manual for additional information on how to enable this function.

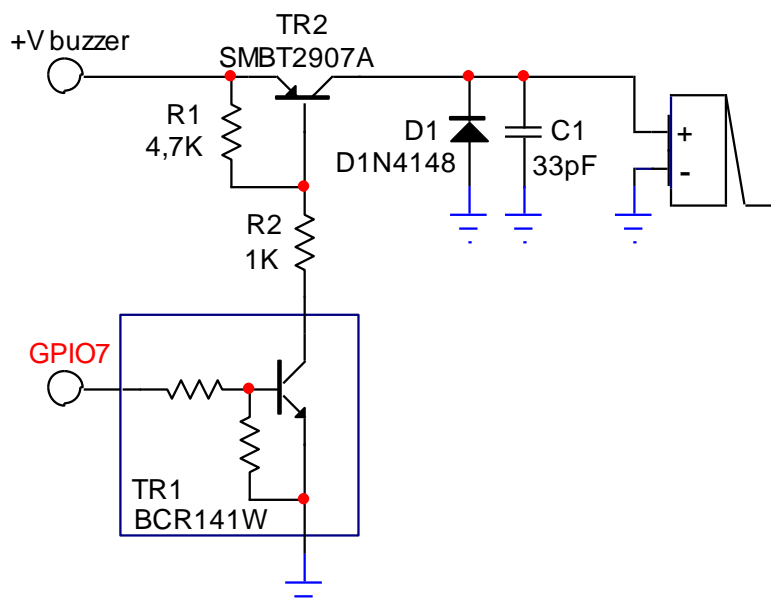
## 11.6. Using the Alarm Output GPIO6

The GPIO6 pad, when configured as Alarm Output, is controlled by the GL865 V3/V3.1 module and will rise when the alarm starts and fall after the issue of a dedicated AT command. This output can be used to controlling microcontroller or application at the alarm time.

## 11.7. Using the Buzzer Output GPIO7

The GPIO7 pad, when configured as Buzzer Output, is controlled by the GL865 V3/V3.1 module and will drive a Buzzer driver with appropriate square waves. This permits to your application to easily implement Buzzer feature with ringing tones or melody played at the call incoming, tone playing on SMS incoming or simply playing a tone or melody when needed.

A sample interface scheme is included below to give you an idea of how to interface a Buzzer to the GPIO7:



### NOTE:

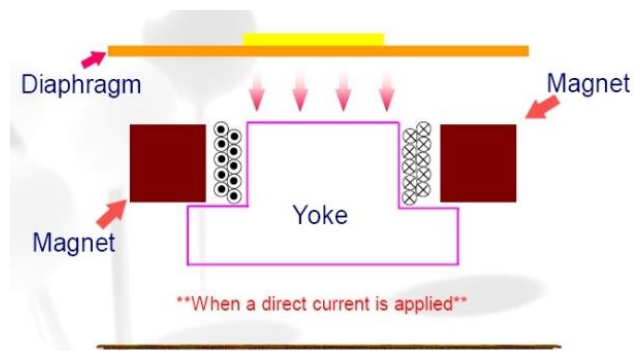
To correctly drive a buzzer a driver must be provided, its characteristics depend on the Buzzer and for them refer to your buzzer vendor.



## 11.8. Magnetic Buzzer Concepts

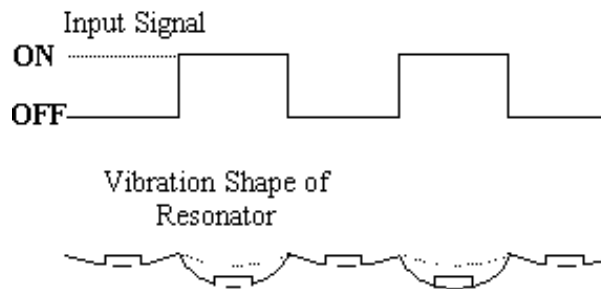
### 11.8.1. Short Description

A magnetic Buzzer is a sound-generating device with a coil located in the magnetic circuit consisting of a permanent magnet, an iron core, a high permeable metal disk and a vibrating diaphragm.



Drawing of the Magnetic Buzzer.

The disk and diaphragm are attracted to the core by the magnetic field. When an oscillating signal is moved through the coil, it produces a fluctuating magnetic field which vibrates the diaphragm at the frequency of the drive signal. Thus the sound is produced relative to the frequency applied.



Diaphragm movement.

## 11.8.2. Frequency Behavior

The frequency behavior represents the effectiveness of the reproduction of the applied signals. Because performance is related to a square driving waveform (whose amplitude varies from 0V to  $V_{pp}$ ), if you modify the waveform (*e.g. from square to sinus*) the frequency response will change.

## 11.8.3. Power Supply Influence

Applying a signal whose amplitude is different from that suggested by the manufacturer, the performance change following the rule “if resonance frequency  $f_o$  increases, amplitude decreases”.

Because resonance frequency depends on acoustic design, by lowering the amplitude of the driving signal the response bandwidth tends to become narrow, and vice versa.

Summarizing:  $V_{pp} \uparrow \rightarrow f_o \downarrow$      $V_{pp} \downarrow \rightarrow f_o \uparrow$

The risk is that the  $f_o$  could easily fall outside of new bandwidth; consequently the SPL could be much lower than the expected.



### WARNING:

It is very important to respect the sense of the applied voltage: never apply to the “-” *pin* a voltage more positive than the “+” *pin*: if this happens, the diaphragm vibrates in the opposite direction with a high probability to be expelled from its physical position. This damages the device permanently.

## 11.8.4. Working Current Influence

In the component data sheet you will find the value of MAX CURRENT: this represents the maximum average current that can flow at nominal voltage without current limitation. In other words it is not the peak current, which could be twice or three times higher. If driving circuitry does not support these peak values, the SPL will never reach the declared level or the oscillations will stop.



## 11.9. STAT LED Indication of network service availability

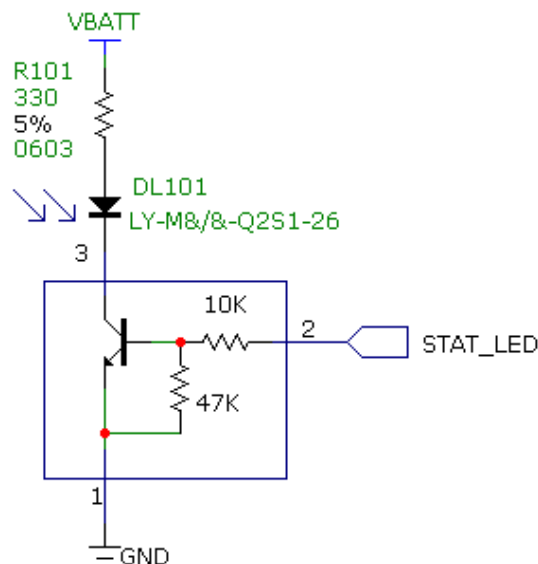
The STAT\_LED pin status shows information on the network service availability and Call status.

In the GL865 V3/V3.1 modules, the STAT\_LED usually needs an external transistor to drive an external LED.

Therefore, the status indicated in the following table is reversed with respect to the pin status.

LED status	Device Status
Permanently off	Device off
Fast blinking (Period 1s, Ton 0,5s)	Net search / Not registered / turning off
Slow blinking (Period 3s, Ton 0,3s)	Registered full service
Permanently on	a call is active

A schematic example could be:





## 12. DAC and ADC section

### 12.1. DAC Converter

#### 12.1.1. Description

The GL865 V3/V3.1 provides a Digital to Analog Converter. The signal (named DAC\_OUT) is available on pin **15** of the GL865 V3/V3.1.

The on board DAC is a 10 bit converter, able to generate an analogue value based on a specific input in the range from 0 up to 1023. However, an external low-pass filter is necessary

	Min	Max	Units
Voltage range (filtered)	0	1.8	Volt
Range	0	1023	Steps

The precision is 10 bits so, if we consider that the maximum voltage is 2V, the integrated voltage could be calculated with the following formula:

$$\text{Integrated output voltage} = (2 * \text{value}) / 1023$$

DAC\_OUT line must be integrated (for example with a low band pass filter) in order to obtain an analog voltage.



### 12.1.2. Enabling DAC

An AT command is available to use the DAC function.

The command is: **AT#DAC=** [*<enable>* [, *<value>*]]

*<value>* - scale factor of the integrated output voltage (0..1023 - 10 bit precision)  
it must be present if *<enable>=1*

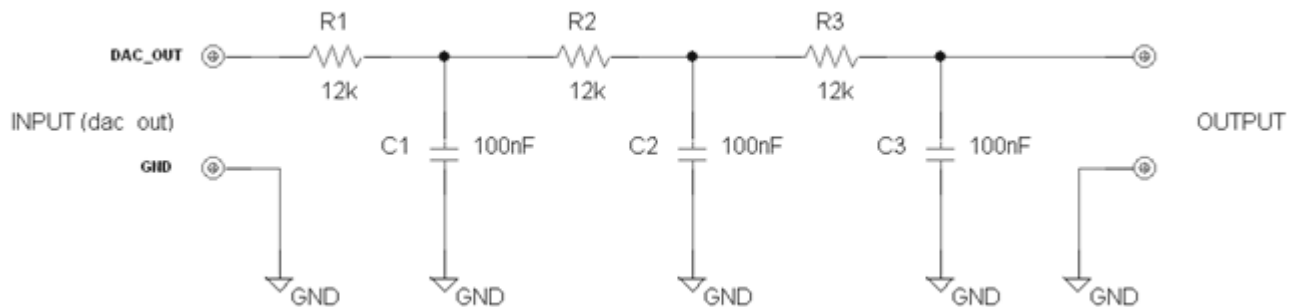
Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.



**NOTE:**

The DAC frequency is selected internally. D/A converter must not be used during POWERSAVING.

### 12.1.3. Low Pass Filter Example



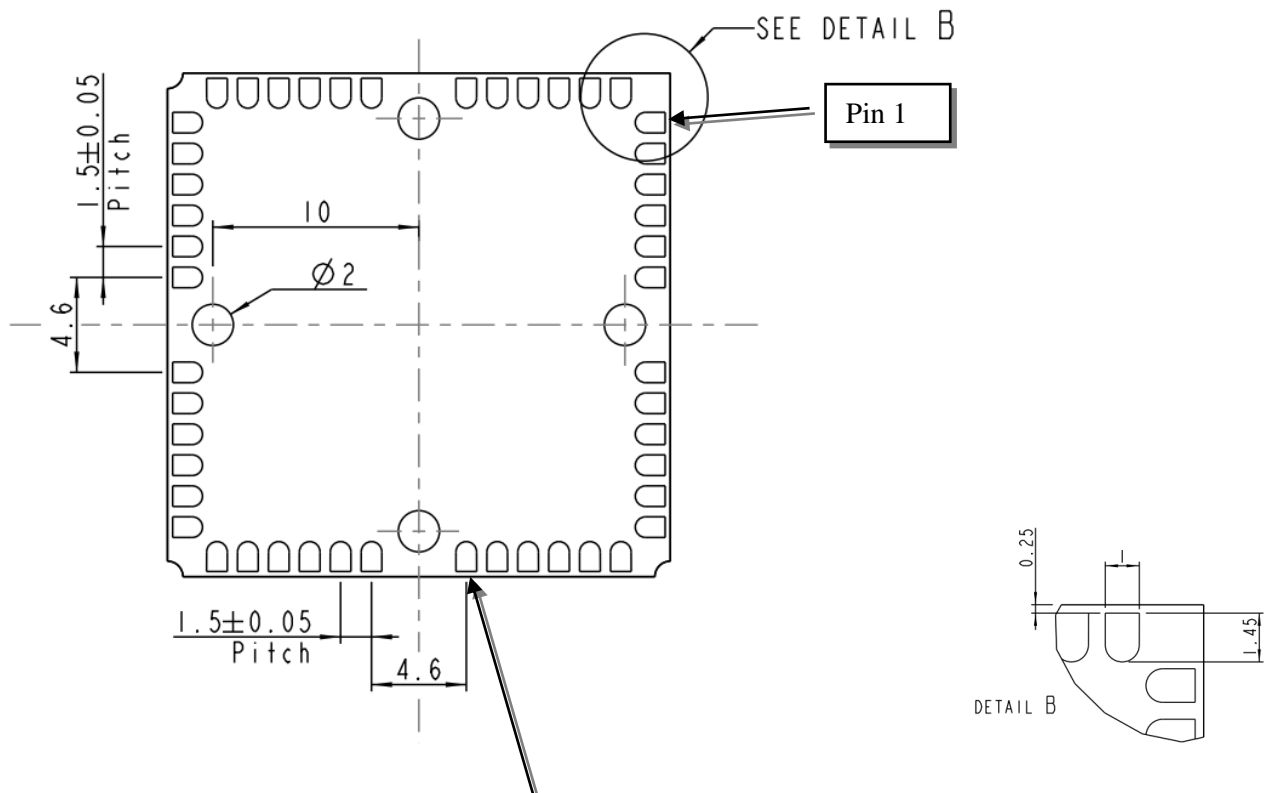


## 13. Mounting the GL865 V3/V3.1 on your Board

### 13.1. General

The GL865 V3/V3.1 modules have been designed to be compliant with a standard lead-free SMT process.

### 13.2. Module finishing & dimensions



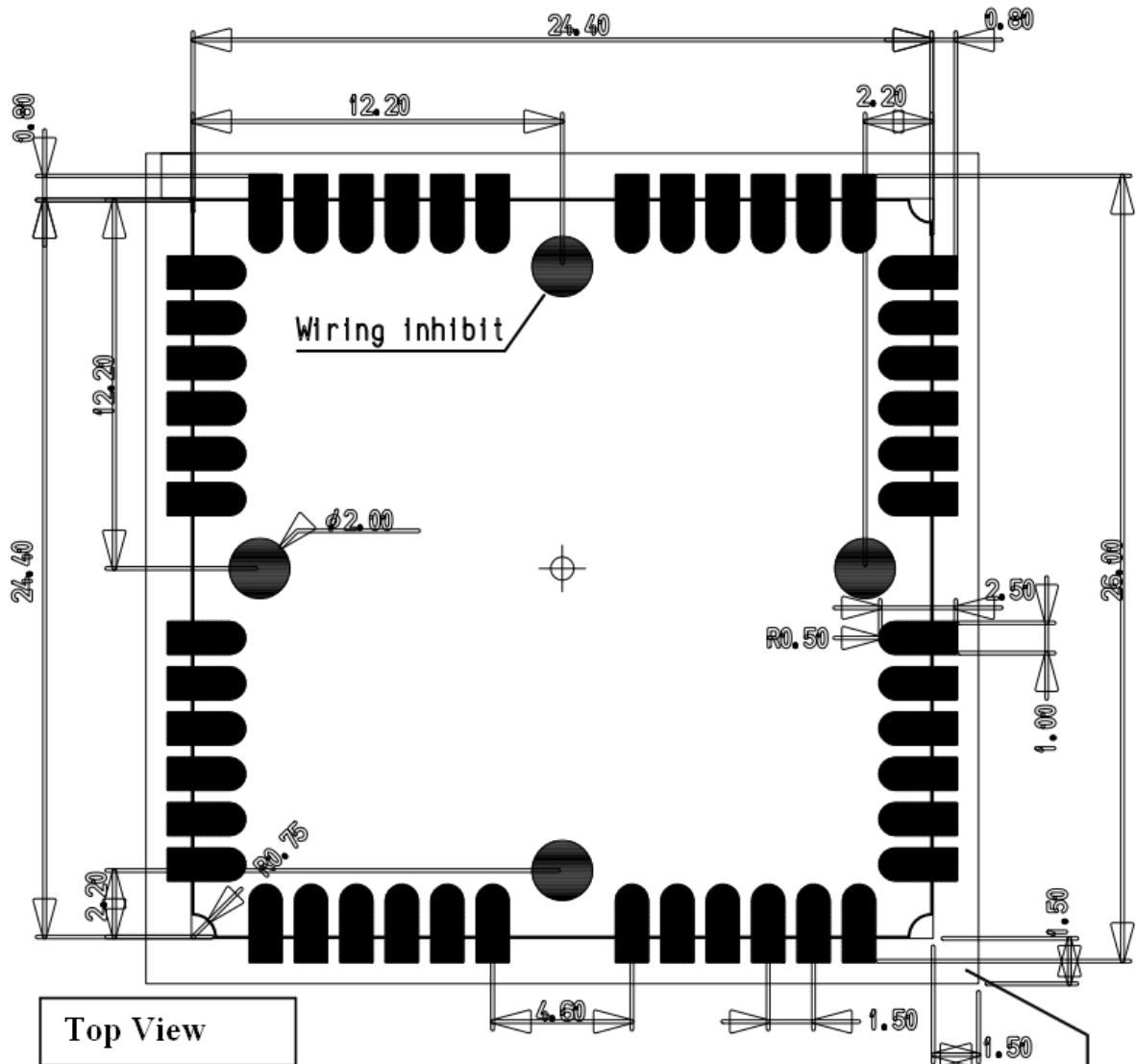
**Lead-free Alloy:**  
Surface finishing Ni/Au for all solder pads

**Bottom View**

**Dimensions in mm**



### 13.3. Recommended foot print for the application



In order to easily rework the GL865 V3/V3.1 is suggested to consider on the application a 1.5 mm placement inhibited area around the module.

It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

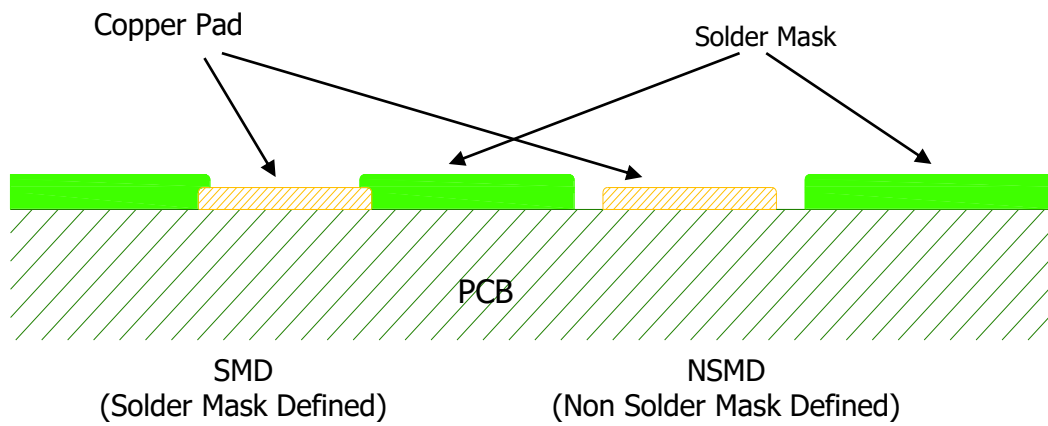
### 13.4. Stencil

Stencil's apertures layout can be the same of the recommended footprint (1:1), we suggest a thickness of stencil foil  $\geq 120\mu\text{m}$ .

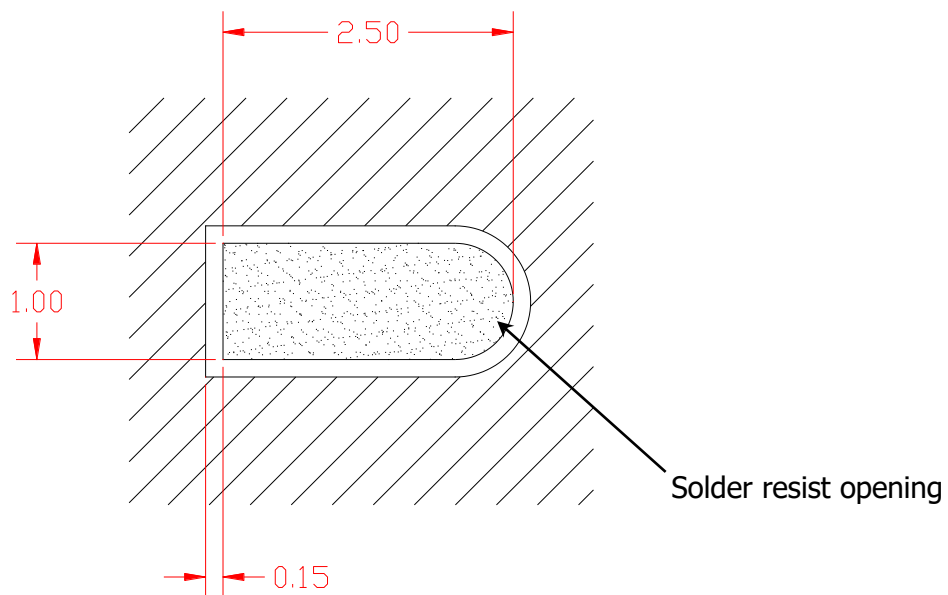


### 13.5. PCB pad design

Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.



### 13.6. Recommendations for PCB pad dimensions (mm):



It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal of the pad itself (see following figure).





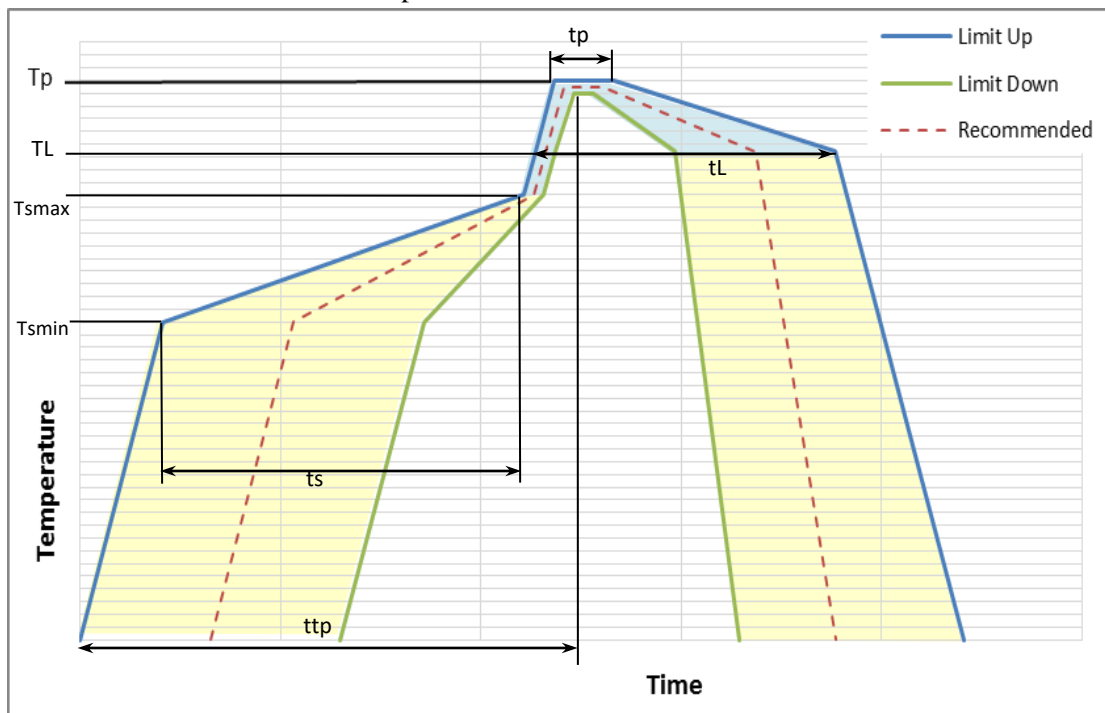
### 13.7. Solder paste

	Lead free
Solder paste	Sn/Ag/Cu

We recommend using only “no clean” solder paste in order to avoid the cleaning of the modules after assembly.

### 13.8. GL865 V3/V3.1 Solder reflow

Recommended solder reflow profile



Profile Feature	Pb-Free Assembly
Average ramp-up rate (TL to TP)	3°C/second max
Preheat	
– Temperature Min (T <sub>min</sub> )	150°C
– Temperature Max (T <sub>max</sub> )	200°C
– Time (min to max) (ts)	60-180 seconds
T <sub>max</sub> to TL	
– Ramp-up Rate	3°C/second max
Time maintained above:	
– Temperature (TL)	217°C
– Time (tL)	60-150 seconds
Peak Temperature (T <sub>p</sub> )	245 +0/-5°C
Time within 5°C of actual Peak Temperature (t <sub>p</sub> )	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature (t <sub>tp</sub> )	8 minutes max.



**NOTE:**

All temperatures refer to topside of the package, measured on the package body surface



**WARNING:**

The GL865 V3/V3.1 module withstands one reflow process only.

## 13.9. Debug of the GL865 V3/V3.1 in production

To test and debug the mounting of the GL865 V3/V3.1, we strongly recommend foreseeing test pads on the host PCB, in order to check the connection between the GL865 V3/V3.1 itself and the application and to test the performance of the module connecting it with an external computer. Depending by the customer application, these pads include, but are not limited to the following signals:

- TXD
- RXD
- RTS
- RESET\*
- GND
- VBATT
- TX\_AUX
- RX\_AUX
- PWRMON



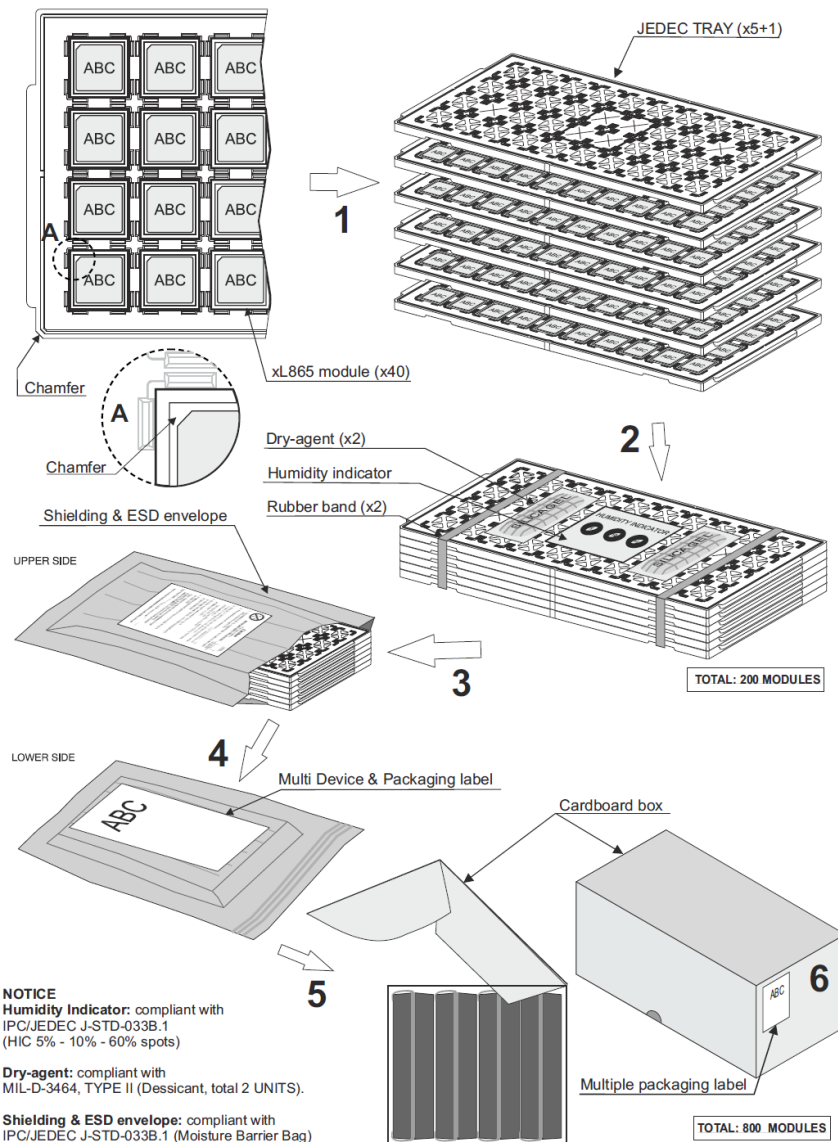
## 14. Packing system

Is possible to order in two packaging system:

- Package on tray
- Package on reel

### 14.1. Packing on tray

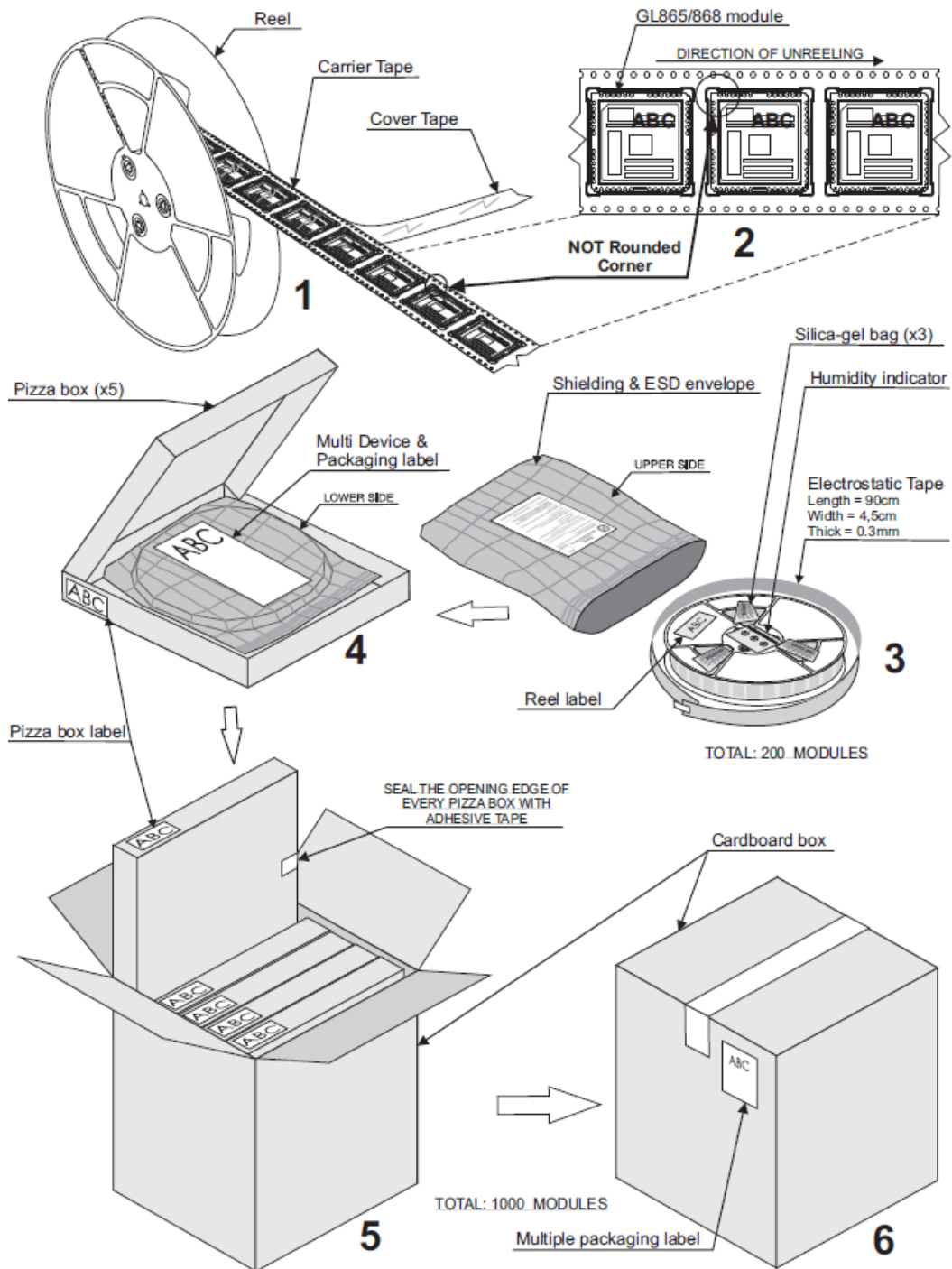
The GL865 V3/V3.1 modules are packaged on trays of 40 pieces each. These trays can be used in SMT processes for pick & place handling.



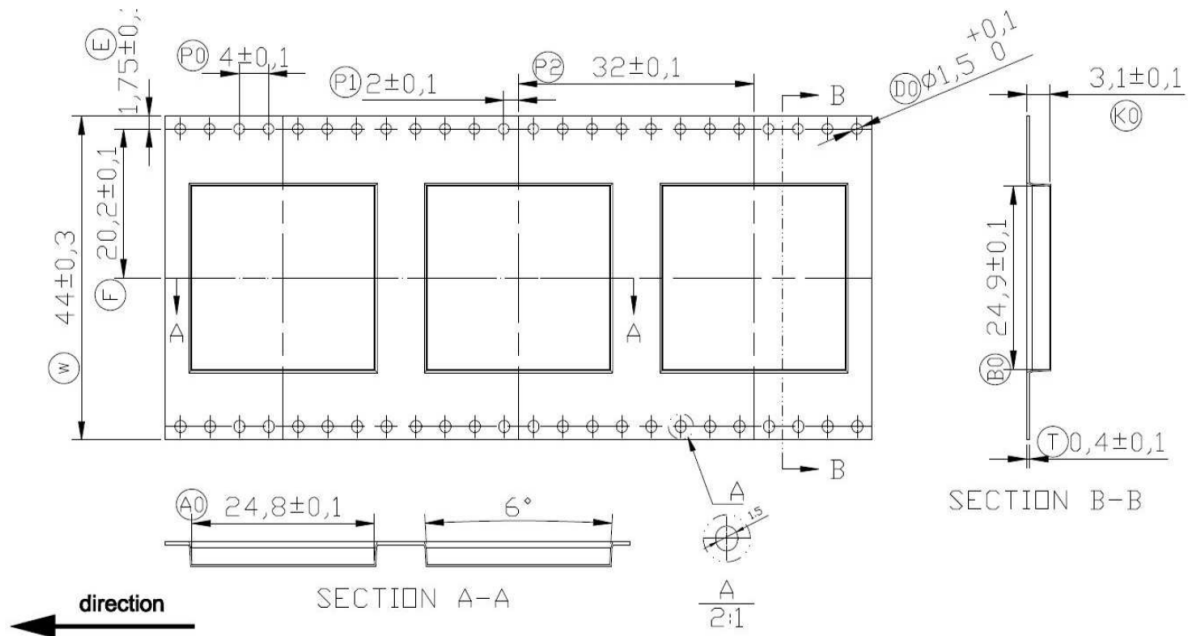


## 14.2. Packing on reel

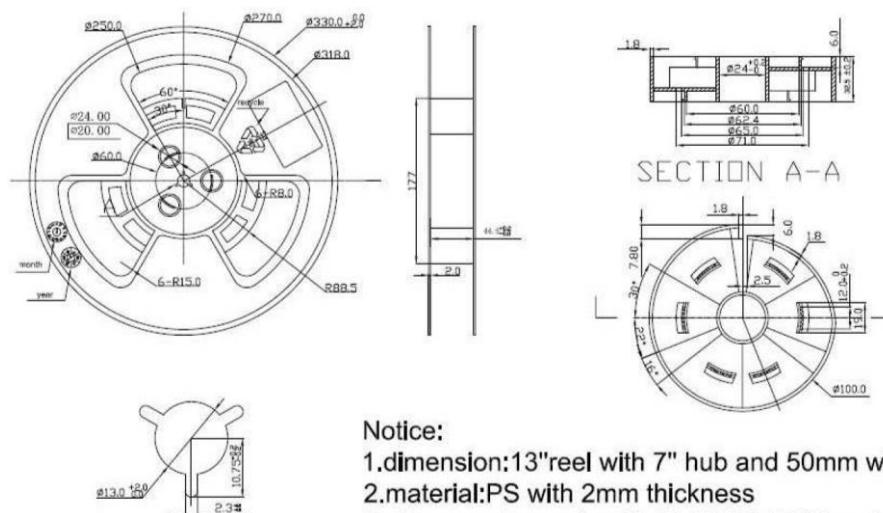
The GL865 V3/V3.1 can be packaged on reels of **200** pieces each. See figure for module positioning into the carrier.



### 14.2.1. Carrier tape detail



### 14.2.2. Carrier tape detail



**Notice:**  
 1.dimension:13"reel with 7" hub and 50mm width  
 2.material:PS with 2mm thickness  
 3.other:must comply with RoHS/REACH and other industry standard





## 15. Conformity Assessment Issues

### FCC/IC Regulatory notices

#### Modification statement

Telit has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

*Telit n'approuve aucune modification apportée à l'appareil par l'utilisateur, quelle qu'en soit la nature. Tout changement ou modification peuvent annuler le droit d'utilisation de l'appareil par l'utilisateur.*

#### Interference statement

This device complies with Part 15 of the FCC Rules and Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

*Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.*

#### Wireless notice

This equipment complies with FCC and IC radiation exposure limits set forth for an uncontrolled environment. The antenna should be installed and operated with minimum distance of 20 cm between the radiator and your body. Antenna gain must be below:

Frequency band	Antenna gain
GSM 850	6.43 dBi
PCS 1900	3 dBi

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

*Cet appareil est conforme aux limites d'exposition aux rayonnements de la IC pour un environnement non contrôlé. L'antenne doit être installé de façon à garder une distance minimale de 20 centimètres entre la source de rayonnements et votre corps. Gain de l'antenne doit être ci-dessous:*

Bande de fréquence	Gain de l'antenne
--------------------	-------------------



GSM 850	6.43 dBi
PCS 1900	3 dBi

*L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur.*

### FCC Class B digital device notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

### Labelling Requirements for the Host device

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labelled to display the FCC ID and IC of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as follows:

Contains FCC ID: RI7GL865Q3  
Contains IC: 5131A-GL865Q3

L'appareil hôte doit être étiqueté comme il faut pour permettre l'identification des modules qui s'y trouvent. L'étiquette de certification du module donné doit être posée sur l'appareil hôte à un endroit bien en vue en tout temps. En l'absence d'étiquette, l'appareil hôte doit porter une étiquette donnant le FCC ID et le IC du module, précédé des mots « Contient un module d'émission », du mot « Contient » ou d'une formulation similaire exprimant le même sens, comme suit :

Contient FCC ID: RI7GL865Q3  
Contient IC: 5131A-GL865Q3  
**CAN ICES-3 (B) / NMB-3 (B)**

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.





